IN THE CLAIMS

Claims 31, 33, and 35 have been amended. A clean copy of the pending claims, as amended, is provided below. Amended claims are indicated so. A marked-up version of the amended claims follows the clean copy.

CLEAN COPY OF PENDING CLAIMS

31. (Three Times Amended) A memory device, comprising:

a memory array;

a register to store at least one bit indicating a suspend status of a write operation for the memory array; and

a control circuit coupled to said memory array and said register, said control circuit to update said register and to control an output of a status signal representing said suspend status of said write operation, and wherein said control circuit includes:

a first state machine to receive commands for accessing said memory array or said register, and

a second state machine coupled to said first state machine and to execute the commands received by said first state machine.

32. (Unchanged) The memory device of claim 31, wherein said write operation represents a byte write operation.

33. (Amended) The memory device of claim 31, wherein said status signal represents a byte write suspend command.

34. (Unchanged) The memory device of claim 31, wherein said control circuit is to receive a status request signal and said register is to output said status signal in response to said status request signal, said status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

35. (Amended) The memory device of claim 31, further comprising:

at least one data input/output coupled to said control circuit, wherein the at least one data input/output is to receive said status request signal from a processor and to provide said status signal to said processor.

36. (Unchanged) The memory device of claim 31, further comprising:

a status output coupled to said register, wherein said status output is to provide a second status signal if said status output is polled, and wherein said second status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

37. (Unchanged) The memory device of claim 31, wherein said status request signal is a read status register command.